ABSTRACT OF THE DISCLOSURE

An arbiter and bus system adopting the arbiter are provided. The bus system includes a bus request receiver, connected to a plurality of master devices, for receiving bus request inputs from the master devices, a priority level extractor for outputting priority level signals indicating predesignated priority levels corresponding to the master devices if the bus requests are input through the bus request receiver, and generating a priority level summation signal indicating all priority levels of the bus requests based on the output priority level signals, a priority output unit for outputting priority levels in order of decreasing priority based on the priority level summation signal generated by the priority level extractor, a priority mapper comprising a master device identifier output unit for extracting identifiers of the master devices submitting bus requests in order to output the extracted master device identifiers corresponding to the priority levels output from the priority output unit, and an arbitration circuit for granting access to a bus, to the master device corresponding to the identifier output from the priority mapper. Accordingly, an arbiter of a priority designation scheme implemented as a simple circuit and a bus system adopting the same arbiter are allowed.